AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. **(currently amended)** A package for electrically connecting to an external printed wiring board and an external electronic device, said package comprising:

a substrate electrically connected to the external printed wiring board;

a semiconductor chip disposed on and electrically connected to the substrate; and

a connector disposed on the substrate for electrically connecting the semiconductor chip to the external electronic device.

2. **(currently amended)** The package as claimed in claim 1, wherein the substrate comprises a plurality of solder balls [[and is]] electrically connected to the semiconductor chip for electrically connecting the semiconductor chip to the external printed wiring board.

3. **(currently amended)** The package as claimed in claim 1, wherein the substrate comprises a plurality of pins [[and is]] electrically connected to the semiconductor chip for electrically connecting the semiconductor chip to the external printed wiring board.

4. (original) The package as claimed in claim 1, wherein the connector is disposed on and electrically connected to the substrate by a surface mount technology process.

5. (original) The package as claimed in claim 1, wherein the semiconductor chip is electrically connected to the substrate by a wire bonding process.

6. (original) The package as claimed in claim 1, wherein the semiconductor chip is electrically connected to the substrate by a flip chip technology process.

7. (original) The package as claimed in claim 1, further comprising a molding compound for encapsulating the semiconductor chip.

8. **(currently amended)** A package for electrically connecting to an external printed wiring board and an external electronic device, said package comprising:

a first substrate;
a first semiconductor chip electrically connected to the first substrate; a second substrate;
a second semiconductor chip electrically connected to the second substrate;
a medium substrate electrically connected to the first substrate and the second substrate; and
a connector electrically connected to the first substrate and the second substrate, wherein the first substrate is electrically connected to the external printed wiring board and the connector is electrically connected to the external electronic device.

9. (original) The package as claimed in claim 8, wherein the first substrate comprises a plurality of solder balls for electrically connecting to the external printed wiring board.

10. (original) The package as claimed in claim 8, wherein the first substrate comprises a plurality of pins for electrically connecting to the external printed wiring board.

11. (original) The package as claimed in claim 8, wherein the first semiconductor chip and the second semiconductor chip are electrically connected to the first and the second substrates by a wiring bonding process, respectively.

12. (original) The package as claimed in claim 8, wherein the first and the second semiconductor chips are electrically connected to the first and the second substrates by a flip chip technology process, respectively.

13. (original) The package as claimed in claim 8, further comprising a first molding compound and a second molding compound for encapsulating the first and second semiconductor chips, respectively.

14. **(new)** A package for electrically connecting to an external electronic device, said package comprising:

a substrate;

a semiconductor chip disposed on and electrically connected to the substrate; and

a connector disposed on the substrate for electrically connecting the semiconductor chip to the external electronic device.

15. **(new)** The package of claim 1, wherein said substrate has opposite upper and lower surfaces;

said substrate further comprising lower conductive elements on the lower surface thereof for electrically connecting the chip to the external printed wiring board;

said substrate further comprising upper conductive elements on the upper surface thereof, said upper conductive elements being electrically connected to said chip and said connector; and

said chip and said connector being physically attached to different regions on the upper surface of said substrate.

16. **(new)** The package of claim 1, further comprising a molding compound encapsulating said chip, wherein

said molding compound and said connector are both disposed on an upper surface of said substrate; and

said connector is positioned completely outside said molding compound.

17. **(new)** The package of claim 1, wherein said connector has a shape of a box including an internal space and an opening on a side of said box.

18. **(new)** The package of claim 8, wherein said first substrate is physically positioned above said medium substrate and said connector which, in turn, are physically positioned above said second substrate.

19. **(new)** The package of claim 8, wherein said first and second substrates are physically separated by a gap and said first and said chips are positioned within said gap.

20. **(new)** The package of claim 8, wherein said connector has a shape of a box including an internal space and an opening on a side of said box.